CLAIMS

1. A method of making an electronic assembly on a substrate comprising:

providing a first set of alignment marks on a substrate;

forming a first group of electronic component features on the substrate using the first set of alignment marks to determine the position of the first group of electronic components on the substrate;

forming a second group of electronic component features on the substrate using the first set of alignment marks to determine the position of the second group of electronic components on the substrate;

forming a second group of alignment marks using the first set of alignment marks to determine the position of the second group of alignment marks on the substrate;

forming a third group of electronic component features on the substrate using the second group of alignment marks to determine the position of the third group of features on the substrate.

2. The method according to claim 1 wherein the second group of electronic component features and the second group of alignment marks are formed in the same process step using the same mask.

3. The method according to claim 1 wherein the third group of electronic component features are a third set of alignment marks.

4. The method according to claim 3 wherein the third set of alignment marks include apertures for aligning the substrate on a final product.

5. The method according to claim 1 wherein the first group of electronic component features includes electrically conductive traces formed on the printed circuit board.

6. The method according to claim 1 wherein the first group of electronic component features includes an insulating layer positioned over electrically conductive traces formed on the printed circuit board.

7. The method according to claim 1 further including forming a fourth group of electronic component features on the substrate prior to forming the third group of electronic component features, the fourth group of electronic components being positioned on the substrate using the first set of alignment marks.

8. The method according to claim 7 wherein the fourth group of electronic components features includes contact pads that are electrically conductive.

9. A method making a circuit assembly on a substrate comprising:

providing a substrate having a first set of alignment marks;

forming a first set of electronic components on the substrate using the first set of alignment marks to position the first set of electronic components on the substrate;

forming a second set of electronic components on the substrate using the first set of alignment marks to position the second set of electronic components on the substrate;

using the same mask that was used to form the second set of electronic components, also forming a second set of alignment marks so that the second set of alignment marks are assured of being a known distance from the second set of electronic components within the tolerances permitted on a single mask;

forming an aperture in the substrate using the second set of alignment marks such that the position of the aperture relative to the second set of electronic components is more precise than it is with respect to the first set of electronic components.

10. The method according to claim 9 wherein the alignment structure is an aperture extending through the substrate, the aperture being provided to align a circuit board with the second set of electronic components.

11. The method according to claim 9 wherein the second set of electronic components is a set of contact pads for being placed in contact with electrodes on a printed circuit board.

12. The method according to claim 9 wherein only a single set of the first set of alignment marks are provided on the substrate and a plurality of sets of the first set of electronic components are formed using the single set of alignment marks.

13. The method according to claim 12 wherein a plurality of the second set of alignment marks are formed on the substrate at spaced locations on the substrate and a plurality of alignment structures are formed adjacent each of the respective second sets of the alignment marks using the set of alignment marks that are the closest to the alignment structures in order to determine the position of the alignment structures on the substrate.

14. The method according to claim 9 wherein the substrate is a flexible electrical connector composed of a plurality of electrically insulating layers and electrically conductive layers.

15. An electronic connector comprising:

a flexible substrate;

a plurality of features positioned on said substrate with reference to a first set of registration guides;

an additional feature positioned on said substrate with reference to said first set of registration guides;

a second set of registration guides positioned on said substrate concurrently with said additional feature;

a second additional feature positioned on said substrate with reference to said second set of registration guides.

16. The connector according to claim 15 wherein said plurality of features includes a plurality of electrically conductive traces.

17. The connector according to claim 15 wherein said plurality of features includes a plurality of electrodes.

18. The connector according to claim 17 wherein each of said plurality of electrodes is in electrical contact with a corresponding one of said plurality of electrically conductive traces.

19. The connector according to claim 17 wherein a plurality of micro-pads are positioned on each of said plurality of electrodes.

20. The connector according to claim 19 wherein said plurality of micro-pads comprises said additional feature.

21. The connector according to claim 15 wherein said additional feature and said second set of registration guides are formed by plating a conductive metal on said flexible substrate.

22. the connector according to claim 15 wherein said second additional feature is a plurality of alignment holes.

23. The connector according to claim 15 wherein said concurrent positioning of said additional feature and said second set of registration guides results in a fixed and known positional relationship between the additional feature and the second set of registration guides.

24. The connector according to claim 23 wherein said positioning of said plurality of features with reference to said first set of registration guides results in a positional relationship fixed within known tolerances between any two of said plurality of features.

25. The connector according to claim 24 wherein said positional relationship between said additional feature and said second additional feature is fixed and known with a high degree of confidence as compared to said positional relationship between any two of said plurality of features.